Competent Fetch Select Adder using 0.12µm Expertise for Low Power Applications

K SRINIVAS RAJU
M. Tech. (ECE)
Department of Electronics and Communication Engineering
Vijay Rural Engineering College, Nizamabad.
Telangana (India)

DR. B.R.VIKRAM
M. E., Ph. D.
Professor in ECE
Department of Electronics and Communication Engineering
Vijay Rural Engineering College, Nizamabad.
Telangana (India)

Abstract:
Most of the VLSI applications, such as DSP, image and video processing, and microprocessors use carry select adder (CSLA) for arithmetic functions. From the structure of regular SQRT CSLA, still there is possibility to obtain better design in which optimization of area, power are to be major concentrations along with high speed performance. One of the existing solutions used in SQRT CSLA is replacement of second level RCA by BEC. Though increases the performance, very less percentage of improvement in reduction of area and power dissipation. And also the existing adder with BEC technique is not suitable for low power applications. Hence this paper proposes Special Hardware using Multiplexers (SHM) design in place of second level RCA. It is observed from the results that the area and power dissipation are reduced at comparable percentages with respect to the RCA and BEC techniques. When SHM is used at the second level of second block in 16-bit SQRT CSLA, observed that area is reduced by 13.5% and power dissipation is reduced by 6.4%. This proposed logic is designed in transistor level using 0.12µm technology in the Micro wind tool.

Keywords: *Architecture, Carry select adder (CSLA), High speed, Power dissipation, Regular SQRT CSLA, Transistor Level*

1. Introduction

Propose of Several Low power VLSI circuit with less area and high speed has become a main concern for digital designers. Building low power VLSI systems has emerged as highly in demand because of the fast growing technology in mobile communications and computation. The battery technology does not advance at the same rate as microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints such as high speed, high throughput, small silicon area, and at the same time, low power consumption. So building low power, high performance adder cells are of great interest [1]-[5]. To reduce the power and area requirements of the computational complexities, the size of transistors are shrunk into the deep sub-micron region [6] and predominantly handled by process engineering.

There are several Adder designs have been proposed to reduce the power consumption. Logic minimization not only results in better system throughput but also results in low power

consumption designs. For low power results it is always advisable to use CMOS technology in which the power dissipation is a complex function of the gate delays, clock frequency, process parameters, circuit topology and structure, and the input vectors applied. Once the processing and structural parameters have been fixed, the measure of power dissipation is dominated by the switching activity (toggle count) of the circuit .The dynamic power is given by,

$$P=1/2 * C_{load} * (V_{dd}^2/T_{cycle}) * E(switching),$$

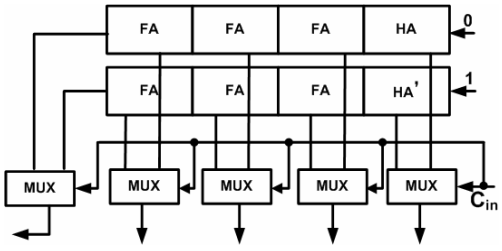
Where C_{load} is the load capacitance of the gate, T cycle is the clock cycle time, E (switching) is the expected number of signal transitions per cycle and V_{dd} is the supply voltage [7].

In digital adders, for speed up the operation Ripple Carry Adder (RCA) is modified as CSLA. To achieve more speed CSLA is replaces by SQRT CSLA. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [8]-[9]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry input Cin=0 and Cin=1, the final sum and carry are selected by the multiplexers(mux) [10]-[14].

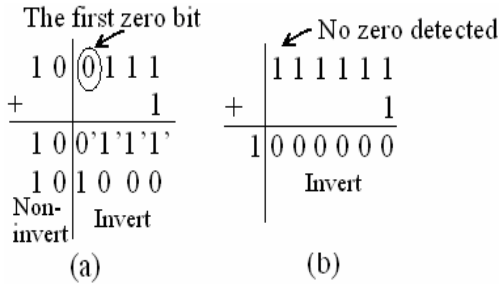
Section II reviews existing logic, section III explains about logic level modification in which replacement of second level RCA with Special Hardware using Multiplexers (SHM). Section III represents results and comparisons. Finally the work is concluded in section IV.

2. Carry-Select Adder and Add-One Circuit

The carry-select adder partitions the adder into several groups, each of which performs two additions in parallel. Therefore, two copies of ripple-carry adder act as carry- evaluation block per select stage. One copy evaluates the carry chain assuming the block carry-in is zero, while the other assumes it to be one. Once the carry signals are finally computed, the correct sum and carry-out signals will be simply selected by a set of multiplexers. A typical block



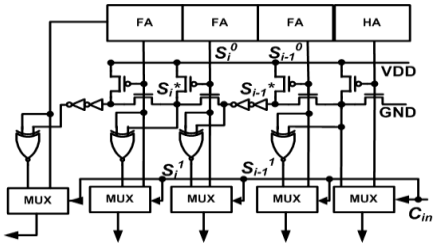
Conventional carry-select adder



Examples for the first zero detection logic

The carry-out signal for the add-one circuit is one if and only if all the sum outputs from the n- bit block are one. As all sums equal one, the first zero detection circuit generates one at the final node. For all the other cases, it generates a zero carry-out. As oppose to using dual RCAs in conventional

CSL, the architecture of contemporary CSL adder comprises a single RCA, a first zero detection and selective complement add-one circuit, and a carry-select multiplexer circuit [3], as shown in Fig



CSL adder with single ripple-carry adder and add-one circuit

3. Existing Logic

In general the complete SQRT CSLA is divided into different blocks. Block size and the number of blocks depend upon the size of SQRT CSLA according to the SQRT technique. From second block onwards, each block contains three different levels, first level is ripple carry adder with input carry zero, second level is ripple carry adder with input carry one and the third level is multiplexer which is used to select one of the ripple carry adders output according to the previous block carries. The disadvantage

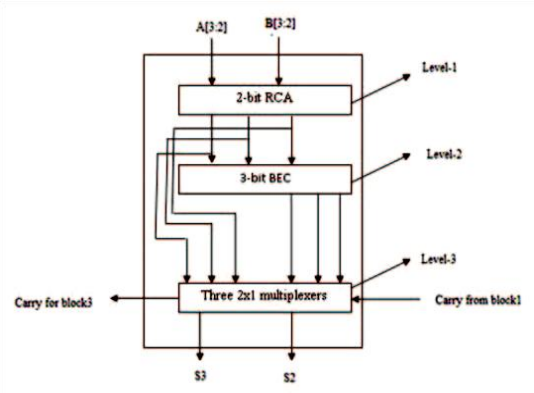


FIG. 1. Second block of SQRT CSLA with BEC in second level RCA

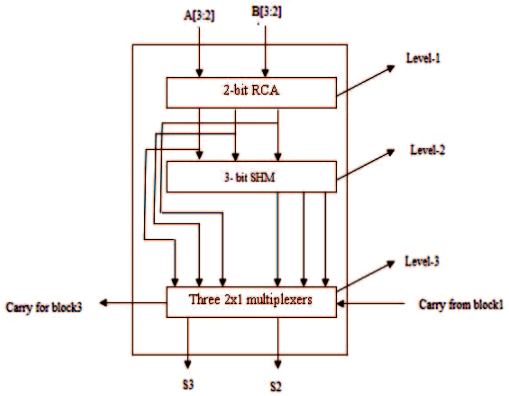


Fig. 2. Second block of SQRT CSLA with SHM in second level RCA

in SQRT CSLA is more area requirement as it uses two levels of RCAs. For achieving better area efficiency [12]-[14] Binary to Excess-1 Converter (BEC) is replaced in the place of RCA with C_{in}=1 in the regular CSLA. To replace n bit RCA an n+1 bit BEC is required.

Second block of 16-bit SQRT CSLA with BEC logic is shown in fig.1. One input of third

level multiplexers is the output of first level RCA and another input is BEC output. This produces the two possible partial results in parallel and the multiplexer is used to select either the BEC output or the direct inputs according to the control signal C_{in} [15].

4. Proposed Logic Implementation

Though BEC technique reduces area and power [15] but not up to considerable amount and also the design is not suitable for sub threshold level modifications.

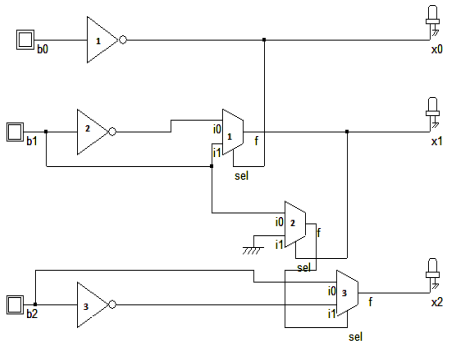


Fig . 3. A 3-bit SHM

$$X0=\overline{b0}$$

$$X1=\overline{X0}.\overline{b1}+X0.b1$$

$$X2=(X1+\overline{b1}).b2+\overline{X1}.b1.\overline{b2}$$

The 16-bit SQRT CSLA using BEC in its second level requires 792 transistors. There is a scope to reduce the number of transistors along with the area reduction and power dissipation reduction by using proposed logic. For the implementation of a 16-bit SQRT CSLA, 736 transistors are required by using proposed logic.

The proposed logic implementation for second level RCA is Special Hardware using Multiplexers (SHM) as shown in fig.2. In this the inputs are applied to first level RCA. And the output of RCA is applied to second level SHM and then to third level multiplexer. Third level multiplexer selects either RCA output or SHM output according to the previous carry.

A simple 3-bit SHM is shown in Fig.3.and logic expressions of SHM shown in below the figure. A simple 3-bit SHM requires 3 multiplexers to implement.. b0, b1, b2 are the inputs to the 3-bit SHM and the x0, x1, x2 are corresponding outputs. SHM will take first level RCA output as input and appends its value by one. 3-bit SHM uses three multiplexers and three inverters. First inverter gives the first output bit x0 basing on input bit b0 and that output will be used as select line for the first multiplexer. First multiplexer passes either second bit b1 or inversion of second bit b1to the output because first inverter output acts like a carry to the second bit. First multiplexer gives the second output bit x1 and that will be used as second multiplexer select line. Basing on x1 output bit and b1 bit second multiplexer generates carry for input bit b2. One input to the second multiplexer is b1 and second input is grounded which will be selected when it is connected as select line to the third multiplexer.

Table 1: Comparison of 3-Bit BEC and 3-Bit SHM

Type of logic	Gates	Number of transistors	Total number of transistors
3- it BEC	2 -XOR 1-AND 1-NOT	24 6 2	32
3-bit SHM	3-MUX 3-NOT	18 6	24

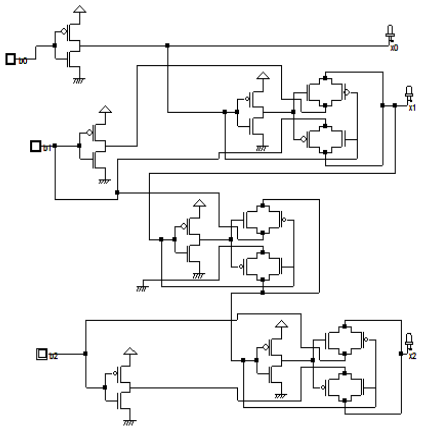


Fig. 4. A 3-bit SHM using CMOS logic

Third multiplexer passes third bit or inversion of third bit to the output according to the previous carry bit. This logic can be extended to any number of bits. It is implemented for second block with two inputs under consideration.

When number of inputs is increased the proposed technique produces more efficient results on large scale. One point to be noticed is despite of the above advantages, delay is increased as carry has to pass 2(n-1) levels in n bit SHM in order to appear at the output. Gate and transistor level Comparisons between 3-bit BEC and 3-bit SHM are shown in Table. I. A 3-bit BEC uses two XOR Gates, one AND Gate and one inverter where as 3-bit SHM uses three multiplexers, three inverters. XOR Gate requires 12.

Table 2: Comparison of Second Level 2- Bit RCA, 3-Bit BEC And 3-Bit SHM Implemented Using CMOS Technology

Logic for Second level	Number of transistors	Critical path delay (ns)	Area (μm^2)	Power dissipation (µw)		
				static	dynamic	total
RCA using CMOS	56	1.900	1342	6.706	42.565	49.271
BEC using CMOS	32	1.200	781	3.269	25.746	29.015
SHM using CMOS	24	2.350	486	3.100	22.843	25.943

Table 3: Comparison between second blocks with BEC and second Block with SHM using CMOS

Design Type	Number of transistors	Critical path delay (ns)	Are a (μm^2)	Power dissipation (µw)		
				static	dynamic	total
RCA-BEC-MUX (CMOS)	106	3.240	346 5	21.00 5	106	127.0 05
RCA-SHM-MUX (CMOS)	98	3.770	299 6	20.13 8	98.624	118.7 62

Transistors and AND Gate requires 6 transistors in CMOS logic. But a single multiplexer requires 6 transistors. From the Table I, it is observed that number of transistors reduced by 25% when compared to existing logic. For large number of inputs SHM is more advantageous. Using CMOS logic 3-bit SHM is implemented and is shown in Fig.4.

5. Results and Comparisons

All the blocks of 16-bit SQRT CSLA, second level of second block such as 3-bit BEC and 3-bit SHM are implemented in Dsch2.6c – Logic Editor and synthesized in Micro wind 2.6a-Layout Editor under 0.12um technology with 1.2 volts as logic high voltage.

The first level of second block is two bit RCA which requires 56 transistors when implemented in CMOS logic. The second level of second block is 3-bit SHM in the proposed logic design; it uses 24 transistors as shown in Fig.4. The third level of second

Block is multiplexer. A simple 2x1 multiplexer uses six transistors in CMOS technology. Block2 needs three 2x1 multiplexers hence eighteen transistors are required for the implementation.

Finally total number of transistors required for the complete block 2 is only 98 when SHM is used. Otherwise it requires 106 Transistors with BEC technique. The number of transistors required for block3 is only 146, for block4 are 194 and for block5 are 242 when SHM is used. Otherwise block3 requires 158, block4 requires210 and block5 requires 262 Transistors with BEC technique. Using SHM for the implementation of a 16 bit SQRL CSLA 736 transistors are required where it requires 792 transistors with BEC technique. Finally the complete second block of16-bit SQRT CSLA with BEC and SHM is implemented using CMOS technology and observed the results and are shown from Table III.

6. Conclusion

In this paper all second level RCA blocks of 16-bit SQRT CSLA are replaced by SHM and the results are compared with existing technique such as BEC. From the comparisons in Table II, it is observed that the variation between 2-bit RCA and proposed technique 3-bit SHM are more comparable such as percentage of utilization of number of transistors is reduced to 57.1%, correspondingly percentage of area required also reduced to 63.7% along with power dissipation reduction advantage of 47.3%. Whereas the variation between 2-bit RCA and existing technique 3-bit BEC is only 42.8% reduction of utilization of number of transistors, 41.8% reduction of area required along with the 41.1% reduction of power dissipation. Finally second block of

16-bit SQRT CSLA is designed using logic level modification such as SHM in place of BEC. From the table.III it is observed that number of transistors is reduced by 7.5%, area is reduced by 13.5% and power is reduced by 6.4%, but critical path delay is increased by 16.3%. Once again it is proved that the tradeoff between area, power and delay, the design is optimized for power and area against to the delay over head. This delay overhead also can be overcome by using various existing low power circuit level modifications

References

1. A good over view of leakage and reduction methods are explained in the book Leakage and reduction in Nanometer CMOS Technologies ISBN 0-387-25737-3.
2. Allipeera, K S., Ahmed Basha,(2012).“An Efficient 64-Bit Carry Select Adder With Less Delay And Reduced Area Application“, International Journal of Engineering Research and Applications(IJERA) .ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 5, September- October 2012, pp.550-554
3. Andamuthu, A. S.Rithanyaa, (2012).”Design Of 128 Bit Low Power and Area Efficient Carry Select Adder”, International Journal of Advanced Research in Engineering (IJARE) Vol 1, Issue 1, 2012 Page 31-34.
4. Bedrij, O.J. (1962). “Carry Select Adder”, IRE Trans. Electron. Comput. pp. 340-344,1962.
5. Ceaing, T.Y. and M. J. Hsaio (1998). “Carry –select adder using single ripple carry adder”, Electron. Lett. Vol.34,no.22,pp.2101-2103, oct.1998
6. Chore, N. M., R. N. Mandavgane, “A survey of low power high speed one bit full adder”, recent advances in networking, VLSI and signal processing, ISSN: 1790-5117. ISBN: 978-960-474-162-5.
7. Kim, Y., and L. S. Kim, (2001). “64-bit carry select adder with reduced area”, Electron. Lett. Vol.37,no.10,pp.614-615, May.2001.
8. Kumar, B Ram and Harish M Kittur, “Low –Power And Area -Efficient Carry Select Adder”, IEEE Transactions on Very Large Scale Integration(VLSI)Systems
9. Kumar, Pardeep (2012). International Journal of Engineering Research and Applications(IJERA) ISSN: 2248-9622 Vol. 2, Issue 6, November-December 2012, pp.599-606
10. Parvathi, M., N. Vasantha, K. Satya Prasad (2012).“Design of High Speed -Low Power-High Accurate (HS-LP-HA) Adder “,ICECT, International conference on Electronics Computer Technology Proceedings, 2012, pp: 523-527, 978-1-4673-1850-1/12@2012, IEEE.
11. Ramkumar, B. H. M. Kittur, and P .M. Kannan,(2010).“ASIC implementation of modified faster carry save adder”, EUR .J. Sci .Res. vol.42, no.1, pp.53-58, 2010.
12. Singh, Arun Prakash., Rohit Kumar (1892).“Implementation of 1-bit Full Adder Using Gate Diffusion Input (GDI) cell”, International Journal of Electronics and Computer Science Engineering J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.
13. Sreedevi, M. and P. Jeno. Paul(2010). “Design and Optimization of a High Performance Low-Power CMOS Flex Cell “, International Journal of Signal System Control and Engineering Application, 2010, vol.3, no.4, pp.65-69. DOI: 10.3923/ijssceapp.2010.65.69.
14. Sreenivasulu, U., T. Venkata Sridhar, (2012).“Implementation of A 4 Bit - ALU Using Low-Power And Area-Efficient Carry Select Adder”, International Conference on Electronics and Communication Engineering, 20th, May 2012, Bangalore, ISBN: 978-93-81693-29-2.
15. Weste, N. and K. Eshraghian, (1993). Principles of CMOS VLSI Design, A System Perspective . Reading, MA: Addison- Wesley, 1993.